REMARKS

The Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow. Claims 1-14 and 21-26 have been rejected, and the Examiner has objected to Claim 1. Claims 1 and 3 have been amended. No new matter has been added. Accordingly, Claims 1-14 and 21-26 are pending in the present application.

This amendment adds, changes and/or deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claim(s) remain under examination in the application, are presented, with an appropriate defined status identifier.

Claim Objections

In Section 3 of the Office Action, the Examiner objected to Claim 1.

Claim 1 has been amended to recite "transferring the trimmed transistor gate pattern to a layer disposed below the trimmed pattern" in accordance with the Examiner's suggestion. Reconsideration and withdrawal of the objection to Claim 1 is respectfully requested.

Claim 3 has also been amended to correct a typographical error included therein. The amendments to Claims 1 and 3 are made for clarity and not for patentability, and are not intended by the Applicants to be limiting.

Claim Rejections – 35 U.S.C. § 103(a)

In Section 5 of the Office Action, Claims 1-14 and 21-26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,139,904 to Auda et al. in view of U.S. Patent No. 6,183,937 to Tsai et al. The Applicants respectfully traverse this rejection.

There is no teaching or suggestion in Auda et al. or Tsai et al. that would motivate one of skill in the art to combine their teachings, and therefore a *prima facie* case of obviousness has not been established with regard to Claims 1-14 and 21-26. The Examiner stated:

> Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to cure the gate pattern as taught by Tsai et al. in the patterning process of Auda et al., since this cure process decompose a conformal surface layer of the patterned photoresist layer while simultaneously forming a patterned photoresist layer having a second linewidth narrower than the first linewidth (column 3, lines 44-49).

As noted in M.P.E.P. 2143, the Examiner has the burden of establishing some suggestion or motivation to modify the reference or to combine reference teachings. It is unclear why the statement cited by the Examiner would motivate one of skill in the art to combine the teachings of Auda et al. and Tsai et al. in the manner taught by the Applicants in the present application. For example, the Examiner has not indicated that there is any teaching or suggestion that would show one of skill in the art how to use the "conformal surface layer decomposed patterned photoresist layer" of Tsai et al. with a reactive ion etching (RIE) process such as that taught by Auda et al., or that it would even be desirable to do so.

As noted by the Federal Circuit, the "factual inquiry whether to combine references must be thorough and searching." *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 60 USPQ.2d 1001 (Fed. Cir. 2001). Further, it "must be based on objective evidence of record." *In re Lee*, 277 F.3d 1338, 61 USPQ.2d 1430 (Fed. Cir. 2002). The teaching or suggestion to make the claimed combination must be found in the prior art, and not in the applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ.2d 1438 (Fed. Cir. 1991). "It is improper, in determining whether a person of ordinary skill would have been led to this combination of references, simply to '[use] that which the inventor taught against its teacher.'" *Lee* (citing *W.L. Gore v. Garlock, Inc.*, 721 F.2d 1540, 1553, 220 USPQ 303, 312-13 (Fed. Cir. 1983)).

The only suggestion to combine the references in the manner recited in Claims 1-14 and 21-26 comes from the Applicants' own disclosure. The Examiner has engaged in hindsight reconstruction by taking elements from otherwise unrelated references in order to reject these claims under 35 U.S.C. § 103(a). Such reconstruction is improper where there is no showing that it is based on knowledge that was within the level of ordinary skill in the art

at the time the claimed invention was made and includes knowledge gleaned only from the Applicant's disclosure. See M.P.E.P. 2145, section X, subsection A.

The rejection of Claims 1-14 and 21-26 cannot be maintained, because there is no motivation to combine the teachings of Auda et al. and Tsai et al. Reconsideration and withdrawal of the rejection of Claims 1-14 and 21-26 is therefore respectfully requested.

Even if there were a proper motivation to combine the teachings of Auda et al. and Tsai et al. (which there is not), Claims 1-14 and 21-26 still would not have been obvious to one of skill in the art at the time of the invention.

Independent Claim 1 recites, among other limitations, "curing the transistor gate pattern with an electron beam" and "trimming the cured transistor gate pattern" (emphasis added). Independent Claim 8 recites, among other limitations, "E-beam irradiating a gate pattern of a photoresist layer" and "trimming the E-beam irradiated gate pattern of the photoresist layer" (emphasis added). Independent Claim 21 recites, among other limitations, "irradiating a portion of the photoresist material with an electron beam to form a gate pattern" and "trimming the gate pattern" (emphasis added).

One nonexclusive example of a trimming operation is described in paragraphs [0039] and [0040] of the present application:

> **[0039]** After E-beam radiation step 12, wafer 20 undergoes resist trimming step 14. Trimming step 14 is preferably a plasma etching step. Wafer 20 is exposed to a plasma etchant to trim or reduce the dimensions of features patterned on the photoresist layer, such as, first and second features 26, 36. The plasma etchant can comprise a variety of plasma etch chemistries, such as, O_2, HBr/O_2, Cl_2/O_2, $N_2/He/O_2$, or N_2/O_2. A variety of standard etching equipment, such as those manufactured by Applied Materials of Santa Clara, California, or Lam Research of Freemont, California, may be utilized to provide the plasma etchant. An exemplary trim/gate stack etch can employ HBr/O2/Ar chemistry for the resist trim, CF4/Ar chemistry for the ARC etch, and a sequence of steps employing one or more of HBr, HeO2, CF3, and CI2 for the poly silicon etch.

> **[0040]** The plasma etchant etches all exposed surfaces between first and second features 26, 36, including the top and side surfaces, to form first and second trimmed gate features 28, 38, respectively (shown in dotted lines in FIGs. 2-4). Because different regions or portions of each of first and second features 26, 36 have different etch rates relative to each other following E-beam radiation step 12 (e.g., vertical etch rate vs. horizontal etch rate), the dimensional reduction of all of the surfaces of first and second features 26, 36 is not the same.

As noted by the Examiner, Auda et al. fails to "teach curing the transistor gate pattern with an electron beam." Auda et al. relates to a "method of producing high resolution and reproducible patterns" and discloses that a "film 17 of a standard photoresist material" is "imaged with UV radiation" to form a "photoresist pattern 17a" that is "placed in reactive ion etching (RIE) equipment and the resist pattern is isotropically eroded to reduce overall dimensions" (Abstract; Column 5, lines 30-63)(emphasis added). There is no teaching or suggestion in Auda et al. to trim a photoresist pattern that has been cured (Claim 1) or irradiated (Claims 8 and 21) with an electron beam.

Tsai et al. also does not teach or suggest trimming a photoresist pattern that has been cured (Claim 1) or irradiated (Claims 8 and 21) with an electron beam. Tsai et al. relates to a "post photodevelopment isotropic radiation treatment method for forming patterned photoresist layer with attenuated linewidth" and discloses the use of a "photoresist material which is susceptible to radiation induced conformal surface layer decomposition and attendant shrinkage" (Column 6, lines 3-6)(emphasis added). Thus, instead of trimming a photoresist pattern that has been cured (Claim 1) or irradiated (Claims 8 and 21) with an electron beam, Tsai et al. discloses the use of a material that shrinks upon exposure to radiation. There is no teaching or suggestion in Tsai et al. to trim such a material.

The rejection of Claims 1-14 and 21-26 cannot be maintained, because at least one limitation of independent Claims 1, 8, and 21 is not taught or suggestion by the combination of Auda et al. and Tsai et al. Reconsideration and withdrawal of the rejection of Claims 1-14 and 21-26 is respectfully requested.

Various claims are also allowable over the combination of Auda et al. and Tsai et al. for additional reasons. For example, Claim 6 recites "wherein the curing step includes exposing the transistor gate pattern to the electron beam having an accelerating voltage in the range of approximately 50-2000 Volts." Claim 10 recites "wherein the electron beam is provided at an accelerating voltage in the range of approximately 50-2000 Volts." Claim 22 recites "wherein the electron beam is provided at an accelerating voltage in the range of approximately 0.5-50 Kv." As noted by the Examiner, Auda et al. fails to "teach curing the transistor gate pattern with an electron beam." While Tsai et al. discloses that "the types of radiation employed . . . include . . . electron radiation" (Column 6, lines 26-34), there is no teaching or suggestion as to the voltage ranges recited in Claims 6, 10, and 22. Such ranges are taught only by Applicants' own disclosure.

Claim 5 recites "wherein the curing step includes exposing the transistor gate pattern to the electron beam having a dose in the range of approximately 100-100000 $\mu C/cm^2$." Claim 9 recites "wherein the E-beam irradiating step uses an electron beam at a dose in the range of approximately 100-100000 $\mu C/cm^2$." As noted by the Examiner, Auda et al. fails to "teach curing the transistor gate pattern with an electron beam." While Tsai et al. discloses that "the types of radiation employed . . . include . . . electron radiation" (Column 6, lines 26-34), there is no teaching or suggestion as to the dosages recited in Claims 5 and 9. Such ranges are taught only by Applicants' own disclosure. Accordingly, Auda et al. and Tsai et al., alone or in combination, do not teach or suggest the subject matter recited in Claims 5 and 9.

Claim 4 recites "wherein the final gate transistor width is in the range of approximately 20-60 nm." Claim 8 recites "the gate width being less than 70 nm." Claim 21 recites "the gate having a width of less than 70 nm." There is no teaching or suggestion in either Auda et al. or Tsai et al. that gate widths such as those recited in Claims 4, 8, or 21 may be achieved using the methods recited in Auda et al. or Tsai et al., either alone or in combination. For example, Auda et al. states that "the method of the present invention allows production of polysilicon line widths of 600 nm with a precision of +/- 180 nm" (Column 10, lines 48-49. Tsai et al. discloses "patterned phororesist line linewidths" of between

approximately 188 and 230 nm (Column 12, Table I). Accordingly, Auda et al. and Tsai et al., alone or in combination, do not teach or suggest the subject matter recited in Claims 4, 8, and 21.

Claim 11 recites "wherein a uniformity of the gate width is 4 to 6 nm over a 3 nm segment." Auda et al. and Tsai et al., alone or in combination, do not teach or suggest the subject matter recited in Claim 11. The Examiner stated:

> The combined teachings of Auda et al. and Tsai et al. substantially teach all aspects of the invention but fail to show . . . wherein the uniformity of the gate width is 4 to 6 nm over a 3 nm segment. Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension.

In contrast to the Examiner's suggestion, producing a gate having a width that has uniformity of 4 to 6 nm over a 3 nm segment is not obvious. As noted in the present application (with emphasis added):

> **[0008]** For example, transistor gates patterned using 193 nm lithography and a typical commercially available photoresist material can have critical dimensions (CDs) of 130-110 nm before the resist trimming process and the final critical dimensions (CDs) of approximately 70-80 nm after the resist trimming process. Any further trimming would typically result in non-uniform widths along the length of the gates, unacceptable consumption of the minimum extension of the gates onto the field isolation regions, (i.e. unacceptably large end of the line pull back) and/or excessive thinning of the gate pattern over topography steps such that pattern transfer to the underlying layer(s) of the wafer is not possible. Such poor trimming results can affect the operating conditions and/or performance of the transistors to the extent that the resist trimming process will become unusable without violating design rules for given technology scaling requirements.

> **[0044]** Preferably, first and second gates 70, 74 have gate widths comparable to width 60. First gate 70 includes a minimum extension 72 onto isolation regions 30 and second gate 74 includes a minimum extension 76 onto isolation regions 30. Each of minimum extensions 72, 76 has a length comparable to extended length 62. The width along the length of each of first and second gates 70, 74 has a variation of less than 1 nm, as opposed to a gate formed from photoresist that was not e-beam eradiated which has a gate width variation along its length of approximately 5 nm. In one embodiment, the local gate width variation is between 4 to 6 nm over a 3 nm gate length (3 sigma). Preferably this variation can be further reduced as technology permits.

Thus, as noted in the present application, the dimensions recited in Claim 11 are not merely a matter of "routine experimentation and optimization" as indicated by the Examiner, but rather represent a non-obvious advance over previous attempts at controlling gate width variations. Accordingly, Auda et al. and Tsai et al., alone or in combination, do not teach or suggest the subject matter recited in Claim 11.

Various other Claims may be allowable for additional reasons. The Applicants expressly reserve the right to set forth additional and/or alternative reasons for patentability and/or allowance in connection with the present application or in any other future proceeding.

* * *

The Applicants believe that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447. If any extensions of time are needed for timely acceptance of

papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 06-1447.

Respectfully submitted,

Date 9/11/03

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